Digital RF Synthesizer: DC to 135 MHz

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See disclaimer[2]

Here, we give a design for a Direct Digital Synthesis (DDS) device to produce Radio Frequency (RF) signals between DC and 135 MHz. The design centers around an AD9852 from Analog Devices (but will also accommodate an AD9854). This design is partially based on that of the evaluation board available from Analog Devices but contains circuits relevant to our laboratory electronics implementation and control system and a redesigned output filter. The digital interface given in this design is relatively simple and can be interfaced with a microprocessor or with the system described on our website `george.ph.utexas.edu/~control`. The PCB layout is located there also, it is a layout design using the software from pcb123. See notes on our website with regard to version.

Digital Side: The digital inputs consist of a 24-bit bus and a strobe bit. The first 16-bits we identify as the data bus and the next 8 as the address bus. This address bus is intended to address many boards, each with a local address set by DIP switches. In the case of this DDS device, the 16-bit 'data bus' is broken up into various parts as discussed below. The address bus uses the first 2 bits (first 4 addresses) to determine the strobe function on the board. The higher 6-bits of the address bus are the board select. If they do not match the address set by the DIP switches then the strobe is rejected and the board does not accept the data. Only when this address matches does the strobe bit cause the 16-bit data bus to be latched.

[1]Please send comments, questions, corrections, insults to *meyrath@physics.utexas.edu*

[2]Disclaimer: The author provides this and other designs on the web as a courtesy. There is no guarantee on this or any other designs presented, use at your own risk. The author also comments that the suggested parts used are not an endorsement of any manufacturer or distributer.

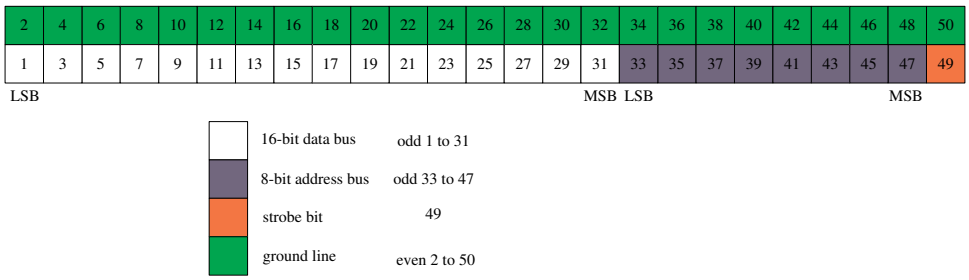

Figure 1: Pin configuration for 50-pin connector.

8-bit address bus			
A1	A0	Option number	Strobe bit function
0	0	Option 0	Latch 16-bit data bus, Master Reset
0	1	Option 1	Latch 16-bit data bus, Load data into DDS buffer
1	0	Option 2	Latch 16-bit data bus, Update output register -or- Load data and Update output (see version 2.0 note below)
1	1	Option 3	Latch 16-bit data bus only
A7 to A2 must match DIP switch settings. DIP switches: ON=0 OFF=1.			

Generally, Option 0, for the master reset is called after power-up of the device.

Programming the DDS: Programming the DDS generally requires several loads of data. The 16-bit data bus is broken up by function as in the table here:

16-bit data bus	
D0 (LSB) to D5	Programming register address in DDS
D6	FSK/BPSK/Hold functions
D7	Shaped Keying function
D8 to D15 (MSB)	8-bit data for referenced programming register

Programming generally consists of multiple loads of data D0 to D5 and D8 to D15 in parallel using address Option 1 to load the DDS registers in the desired locations with the desired values. Then Option 2 is used for an update of the output register in which the DDS uses the previous loaded values to determine the new output characteristics. In the case of Option 2, the D values are unimportant. This is just sending the strobe to the update output. D6 and D7 are used for the named functions above with the address Option 3 or are instead triggered by the external BNC option, see below.

With D0 to D5 as a 6-bit register address location in the DDS, there are 64 memory locations in the DDS (all of which are not used), each 8-bit wide, which may be updated with the Option 1 load method. The address meanings are given in Table IV on page 26 of the AD9852 data sheet. Information on the modes of operation of the device is also given on the data sheet, see pages 15 to 26 for a description. We do not reproduce this information here. Just as a summary, this very impressive device can

operate in the following modes: Single-tone, Frequency Shift Keying (FSK), Ramped FSK, Frequency Chirp, and Binary Phase Shift Keying (BPSK).

Clock Options: The internal PLL clock multiplier of the DDS may be set to any integer between 4 and 20 or not used. This design is intended to run at the maximum frequency of the DDS of 300 MHz. The clock for the DDS can be setup in one of 3 ways. One is to use a crystal (Y1) on the PCB, the clock multiplier must be used and set to $\times 6$ in the case that the 50 MHz crystal suggested on the parts list is used, also, C53 and R19 should be omitted and W15 included, see below. The second option is to use a single ended external clock which enters on the BNC J5, in this case W15 is not used. In this case, the input clock is converted to a differential ECL type by U8. The third option is to use a differential ECL type clock input with BNCs J9 and J10.

Analog Side: Aside from the output options (see below), the analog side consists principally of a pair of filters. The AD9852 has two high speed outputs. Output 1 is the RF (cosine) output and Output 2 is an arbitrary 'control' DAC. The AD9854 which is pin-for-pin compatible has a quadrature RF for Output 2. The filter in this design is a 9th Order 135 MHz Low Pass Elliptic Filter. Which gives a very fast drop off after 135 MHz, below 60 dB stopband begins just above 150 MHz which is the Nyquist frequency. The conceptual schematic is shown in Figure 2 and the frequency transfer function in Figure 3.

Output Options: The output BNCs are J1 to J4 and J6. The 'normal' output setup is labeled (1a) and (1b) in the jumper table below. In this case the two RF (cosine and control) outputs are pass the filters and exit through J1 and J2. Another possibility is to obtain a filtered differential pair for the cosine output on J1 and J2, this is labelled 2 on the jumper table. This also has a special case which can use the DDS's internal comparator to produce an agile digital clock output (J6). And naturally, there is an option for an unfiltered output, whereas the user may add a different filter after the output of the device for desired results.

FSK, BPSK, Hold, Shaped Keying Options: The AD9852 device has a number of extra options for various modulation methods. These are described in detail on the datasheet. This design has the options of having these triggered on the programming bus (slower) or externally (faster). The necessary jumpers are discussed in the table below.

Jumper Options: There are a number of options that may be enabled or disabled by soldering on jumpers labelled `W` on the schematic and the board. These jumpers are acutally $0\,\Omega$ resistors in a 1206 surface mount package.

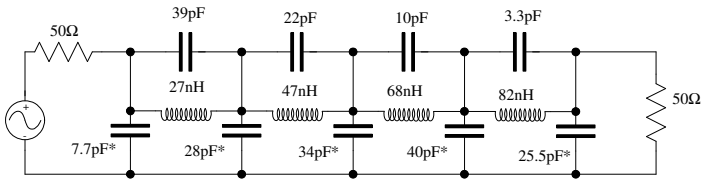

Figure 2: 9th Order 135 MHz Low Pass Elliptic Filter. This filter gives a very fast drop off after 135 MHz, below 60 dB stopband begins just above 150 MHz. Resonances occur for the LC modes at 155.1 MHz, 156.5 MHz, 193.0 MHz, and 306.0 MHz. The starred capacitors to the ground include estimated stray capacitance due to board layout of 2.1 pF, 1 pF, 1 pF, 1 pF, and 3.5 pF left to right, respectively. These values were estimated from pad area at the nodes. Errors in these capacitances principally affect ripple in both the pass band and stop band. Note that the capacitor values given on the circuit diagram at the end are those of the 1206 chip capacitors which are to be attached to the PCB and are all of standard available values. The chip capacitors and inductors also have some small error, generally order 5% or less which can have an effect on the filter transfer characteristics. The inductors used (see parts list) all have a tiny stray capacitance (order 0.3 pF) which adds to that of its parallel capacitor. The theoretical transfer function is plotted in Figure 3.

Option	Jumpers to connect	Jumpers to omit	Other components
Clocks: W6, W7, W15, W16, W17			
(1) Crystal - Y1	W15, W16, W17	W6, W7	omit C53 and R19
(2) Single ended input - J5	W16, W17	W15, W6, W7	
(3) Differential input - J9, J10	W6, W7	W16, W17	
Outputs: W3-W5, W8-W13			
(1a) Filtered RF 1 - J2 single ended	W9, W12	W8, W5, W13	R12 should be 25 Ω
(1b) Filtered RF 2 - J1 single ended	W4, W10	W3, W5, W11	
(2) Filtered RF 1 - J1, J2 differential	W5, W9, W10, W12	W3, W4, W8, W11, W13	R12 should be 50 Ω
(3a) Unfiltered RF 1 - J4	W8	W9, W12, W13	R12 should be 25 Ω
(3b) Unfiltered RF 2 - J3	W3	W4, W5, W10, W11	
(4) Comparator Output - J6	W5, W9, W11, W13	W3, W4, W8, W10, W12	R12 should be 50 Ω
FSK/BPSK/HOLD Input: W2, W18			
(1) From control bus - D6	W2	W18	
(2) External - J8	W18	W2	
Shaped Keying Input: W1, W19			
(1) From control bus - D7	W1	W19	
(2) External - J7	W19	W1	

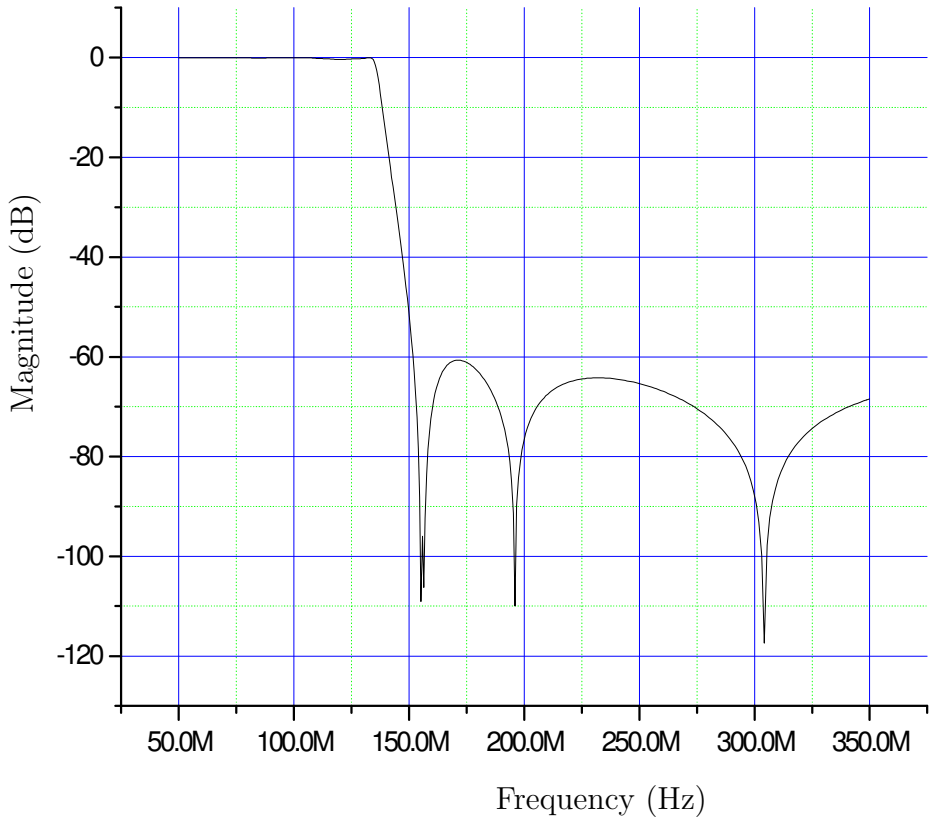

Figure 3: Filter Transfer Function. Theoretical — SPICE plot.

Version 2.0 modifications:

(1) Addition of the inverter before pin 21 of the DDS, to correct the loading problem. Version 1.0 boards use an inverter on a small auxiliary PCB with jumpers.

(2) Addition of the option of sending the update output strobe (pin 20) on the same bus cycle as the load data. In this case, with lower address bits of 01 only the load data is sent for filling the DDS registers, and for 10 load data and update output is sent with a time lag between them. To have this option enabled use W22 and W25 with the additional delay line, omit W23 and W24. To use in the original (version 1.0) configuration, use W23 and W24, omit W22, W25, R23, and C57. If it is preferred to use the internal output update signal, then one may omit both W24 and W25.

(3) Modification of the pads on the bottom of the board for the possibility of clamping the PCB to the box directly below the DDS chip. This also includes the addition of 2-56 through holes near the DDS. Appropriate modification to the box was also made. The holes below the DDS and the voltage regulators were made smaller and more numerous. This requires the use of solder paste rather than any drip solder method from the back. These modifications were done to address the overheating concern of the version 1.0 board and seem to have worked well.

(4) Addition of another single ended clock input on the back of the board and box

labeled J5A and R19A. This is used as a replacement for J5 and R19. One must put in W26 for this option to be used, omit W26 if using the side clock port.

Comments and Improvement Possibilities:

Comment on digital side speed: Although the DDS device digital side may be updated at rate of order 100 MHz, the HC type devices used on the digital side limit the speed to about a quarter of this. However, before this limit, one may find a limit with the ribbon connector and layout. Typically, we operate much slower (order 500 kHz). For some options, such as the FSK, BPSK, Hold, and Shaped Keying functions, there is an available BNC to directly drive these functions with an external source at full speed. For very high speed operation, a slightly modified design involving a high speed FIFO memory located right next to the DDS might be appropriate for a next generation device. TI and Cypress Semi. have many such appropriate memory ICs. In the case of operating at higher frequencies, the delay line for the strobe signal would have to be appropriately modified or removed all together. The various gates between pin 12 of U2 and the strobe inputs of U1 likely produce sufficient delay for the data to settle before strobing.

This design is relatively rudimentary and could likely be specialized for other tasks, such as involving a VCO and PLL type system to produce higher frequencies.

Comment: all options on this design have not been tested.

Soldering Method: We used solder paste (Kester water based solder paste, KE1512-ND from Digikey electronics). The solder paste is applied to the pins and the the backplane of the DDS IC. We also used the solder paste on the voltage regulators. For the solder reflow, we used a standard toaster oven and brought the temperature to about 220°C. Note: the DDS is a moisture sensitive device, so we first baked it out at about 120°C for several hours. See the website:
`http://www.seattlerobotics.org/encoder/200006/oven_art.htm`
for amateur solder paste ideas. The original version required us to fill in the larger holes prior to soldering the ICs. In this version, we simply apply solder paste to the large solder pads and pins for both the DDS and the voltage regulators and did the baking on a steel plate so the solder did not drip out of the holes.

We would like to thank the Kirk Madison boys at UBC for useful discussions on this topic and our co-worker Gabriel Price for constructing most of the synthesizers running our experiment.

Parts			
Qu.	Label	Part #	Manufacturer/Description
1	U1	AD9852ASQ	Analog Devices / Complete DDS 80-LQFP pkg.
2	U2, U12	SN74HC14D	Texas Inst. / Hex schmitt-trigger inverters, 14-SOIC pkg.
1	U3	SN74HC688D	Texas Inst. / 8-Bit Mag. Comp., 20-SOIC wide pkg.
1	U4	CD74HC08M	Texas Inst. / Quad 2-input AND gate, 14-SOIC pkg.
2	U5,U6	CD74HC573M	Texas Inst. / 8-bit Bus Latch, 20-SOIC wide pkg.
1	U7	SN74HC139D	Texas Inst. / 2T04 Decoder 16-SOIC pkg.
1	U8	MC100LVEL16D	ON Semi. / ECL Reciever, 8-SOIC pkg.
3	U9,U10,U11	TPS78633KTTT	Texas Inst. / 3.3V wide band regulator, DDPAK-5.
4	C1,C2,C15,C16		39pF cap, 1206 pkg.
2	C3,C4,C17,C18		22pF cap, 1206 pkg.
2	C5,C6		10pF cap, 1206 pkg.
2	C7,C8		3.3pF cap, 1206 pkg.
2	C9,C10		5.6pF cap, 1206 pkg.
2	C11,C12		27pF cap, 1206 pkg.
2	C13,C14		33pF cap, 1206 pkg.
5	C29-C31,C52,C53		10nF cap, 1206 pkg.
1	C55, C57		120pF cap, 1206 pkg.
1	C19	T491X477K006AS	Kemet / SMD Tant Cap 6.3V 470 μF 'X' pkg.
6	C20-C25	T491B106K006AS	Kemet / SMD Tant Cap 6.3V 10 μF 'B' pkg.
13	C26-C28,C43-C51,C56		0.1 μF cap, 1206 pkg.
11	C32-C41,C54 †		0.1 μF cap, 0603 pkg.
2	L1,L2	KQ1008LTE27NJ	KOA Speer / 27nH 5%, 1008 pkg.
2	L3,L4	KQ1008LTE47NJ	KOA Speer / 47nH 5%, 1008 pkg.
2	L5,L6	KQ1008LTE68NG	KOA Speer / 68nH 2%, 1008 pkg.
2	L7,L8	KQ1008LTE82NG	KOA Speer / 82nH 2%, 1008 pkg.

† These capacitors are not labelled on the PCB, they are the small pads near U1.

Parts			
Qu.	Label	Part #	Manufacturer/Description
1	R1, R23		1.0 kΩ 1260 pkg resistor.
6	R2-R7		10 kΩ 1260 pkg resistor.
1	R8		3.9 kΩ 1260 pkg resistor.
1	R9		1.3 kΩ 1260 pkg resistor.
2	R10,R12		24.9 Ω 1% 1260 pkg resistor.
8	R11,R13,R14, R17-R19, R21,R22		49.9 Ω 1% 1260 pkg resistor.
2	R15,R16		100 Ω 1260 pkg resistor.
1	R20		2 kΩ 1260 pkg resistor.
?	W1-W26		0 Ω (jumper) 1260 pkg resistor.
1	S1	SDA06H1KD	ITT Ind. 6 pos top slide DIP switch, 12-DIP pkg.
10	J1-J10, J5A	31-203-RFX	Amphenol RF / Panel mount BNC receptacle
1	J11	1-103308-0	AMP, Tyco Elect. / 50 pos. header.
1	J12	70543-0002	Molex / 3 pin vertical header power conn.
1		50-57-9403	Molex / 3 pin mate housing.
		16-02-0102	Molex / female crimp pins.
1	Y1 ††	XOSM-573	Vishay Dale / 50 MHz clock oscillator

Quantity is per board, label is on the PCB, part # is manufacturer number. Most parts obtained from *www.mouser.com*, *www.digikey.com*, or *www.alliedelec.com*. ††Crystal oscillator is optional, if used, the internal PLL clock multiplier of the DDS must be used and set to ×6, also, C53 and R19 should be omitted, see text.

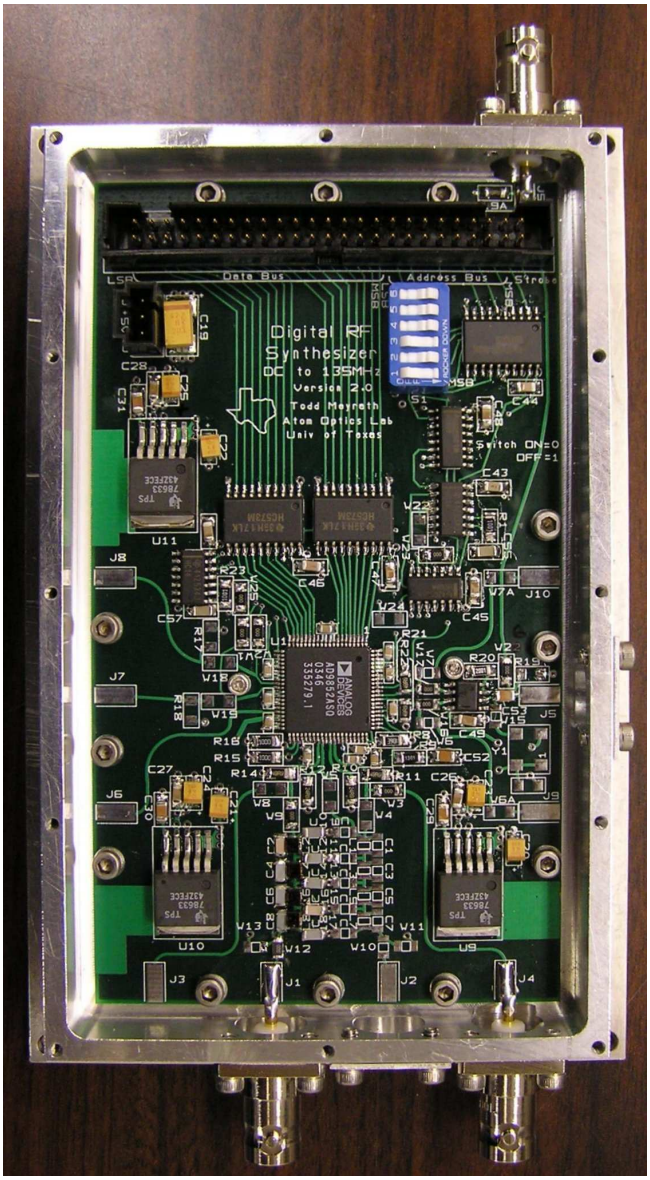

Figure 4: Version 2.0 Board (in a modified Version 1.0 box). This board uses the filter option for the RF output, the unfiltered for the control DAC output, and clock input on the rear.

DIGITAL RADIO FREQUENCY SYNTHESIZER

Version 2.0

Direct RF output frequency range: DC to 135MHz

Todd Meyrath
CNLD, Atom Optics
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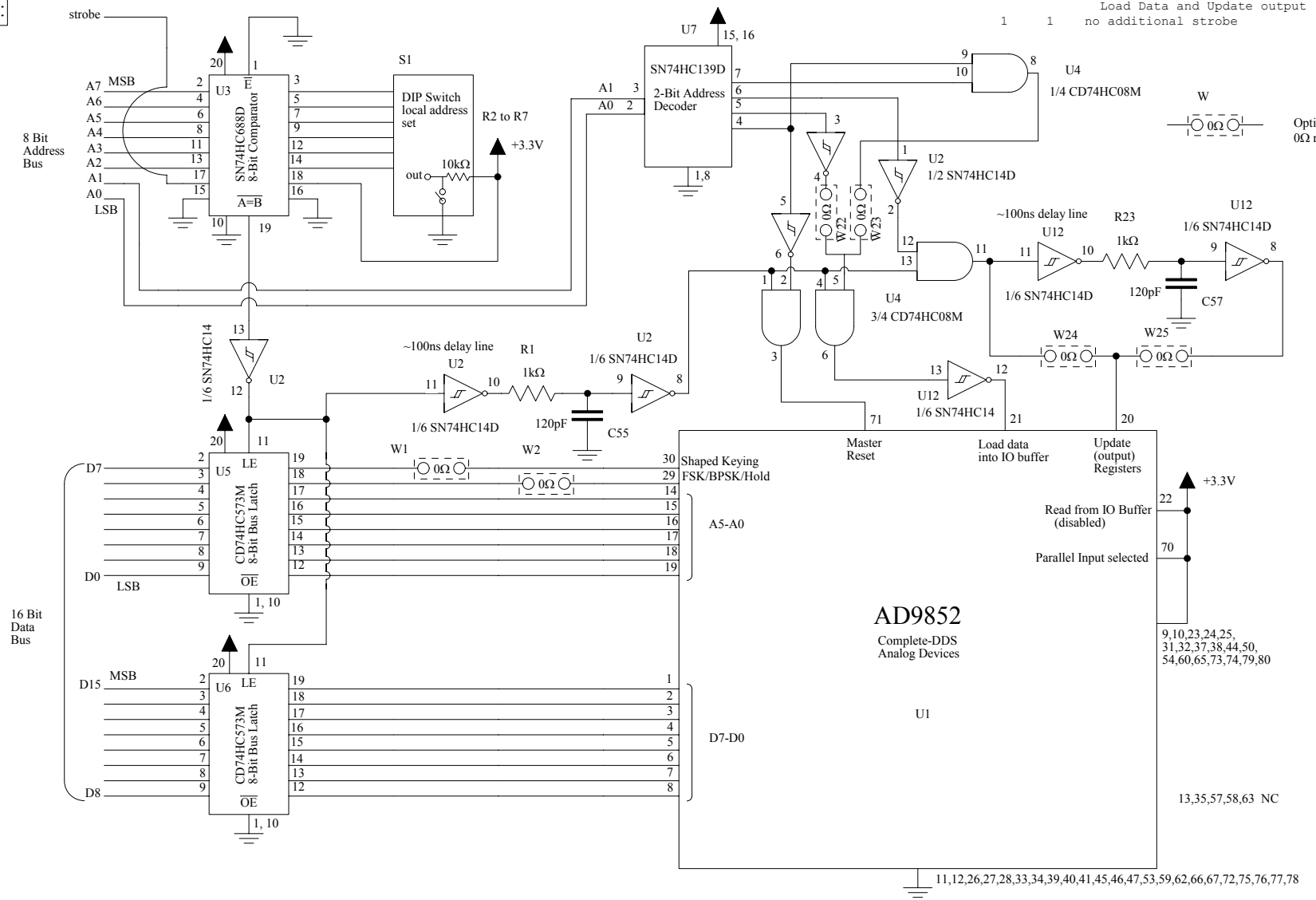
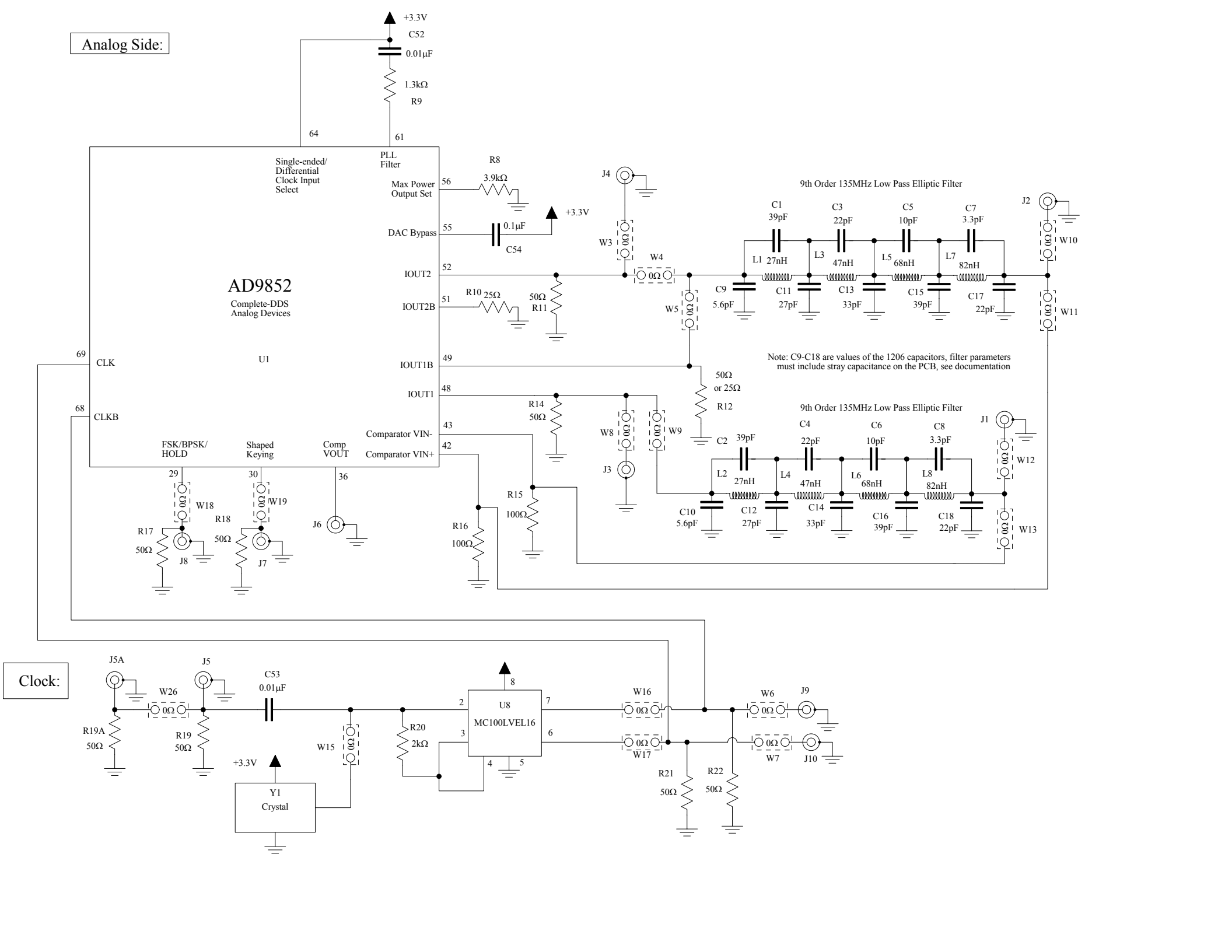
July 2005

Based on AD9852 from Analog Devices.

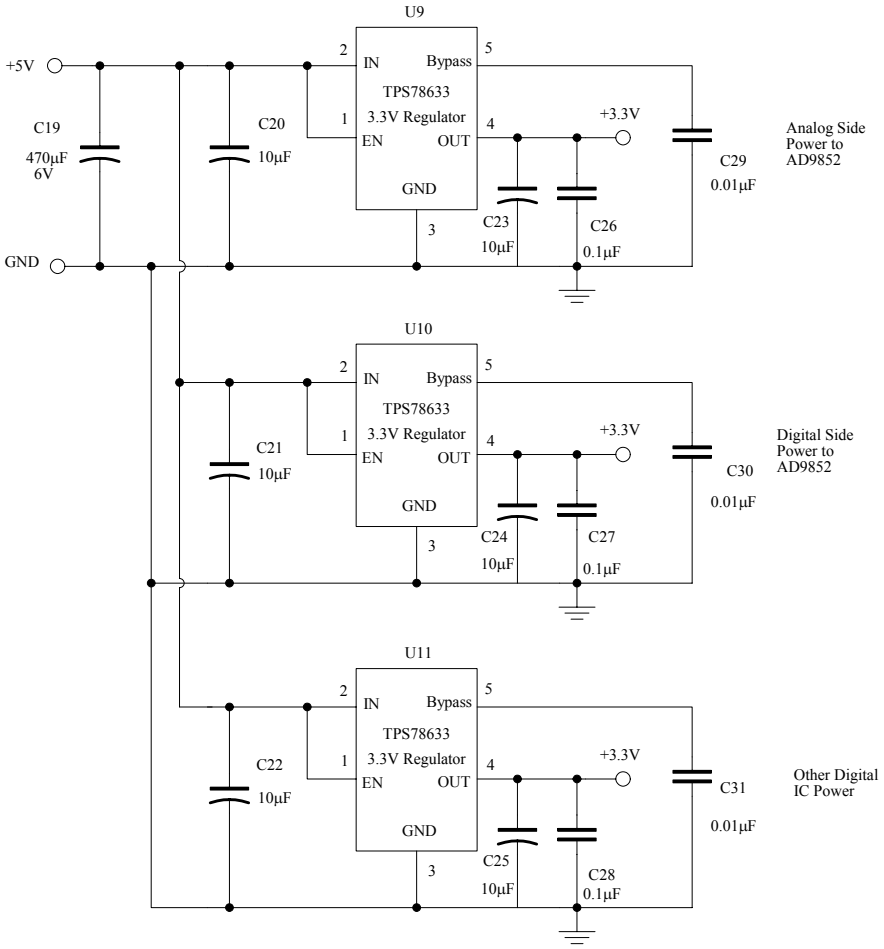
```
Address for board set with DIP switches
A7..A2 A1 A0, lowest bits give function
Additional Strobe Bit:
address:      function:
 A1     A0
  0      0    Master Reset
  0      1    Load Data to buffer
  1      0    Update output register (W22) -or-
                Load Data and Update output (W23)
  1      1    no additional strobe
```

Digital Side:

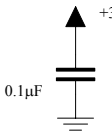



Analog Side:
+3.3V
C52
0.01µF
1.3kΩ
R9
64
61
Single-ended/
Differential
Clock Input
Select
PLL
Filter
AD9852
Complete-DDS
Analog Devices
U1
CLK
CLKB
IOUT2
IOUT2B
IOUT1B
IOUT1
Comparator VIN-
Comparator VIN+
Max Power
Output Set
DAC Bypass
FSK/BPSK/
HOLD
Shaped
Keying
Comp
VOUT
R8
3.9kΩ
56
55
52
51
49
48
43
42
29
30
36
69
68
0.1µF
C54
R10 25Ω
50Ω
R11
J4
W3
W4
W5
W8
W9
J3
R14
50Ω
R15
100Ω
R16
100Ω
50Ω
or 25Ω
R12
W18
W19
R17
50Ω
R18
50Ω
J8
J7
J6
9th Order 135MHz Low Pass Elliptic Filter
C1
39pF
L1 27nH
C3
22pF
L3
47nH
C5
10pF
L5 68nH
C7
3.3pF
L7
82nH
C9
5.6pF
C11
27pF
C13
33pF
C15
39pF
C17
22pF
J2
W10
W11
Note: C9-C18 are values of the 1206 capacitors, filter parameters
must include stray capacitance on the PCB, see documentation
9th Order 135MHz Low Pass Elliptic Filter
C2
39pF
C4
22pF
C6
10pF
C8
3.3pF
L2
27nH
L4
47nH
L6 68nH
L8
82nH
C10
5.6pF
C12
27pF
C14
33pF
C16
39pF
C18
22pF
J1
W12
W13
Clock:
J5A
J5
W26
C53
0.01µF
R19A
50Ω
R19
50Ω
+3.3V
Y1
Crystal
W15
R20
2kΩ
U8
MC100LVEL16
8
2
3
4
5
7
6
W16
W17
R21
50Ω
R22
50Ω
W6
J9
W7
J10

Supply Regulator and Bypass circuits:



Bypass Capactors: on each supply pin for all ICs



U1: C32-C42
U2: C43
U3: C44
U4: C45
U5: C46
U6: C47
U7: C48
U8: C49
U12: C56

Y1: C51

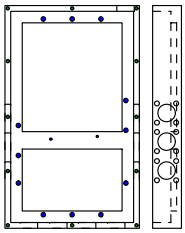
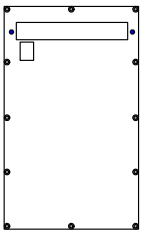
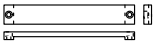
Box for Digital RF Synthesizer (Version 2)

Todd Meyrath
Atom Optics Lab
Univ of Texas
1-0883

Drawing's scale 1:1

Material: Aluminum, all parts

1:5

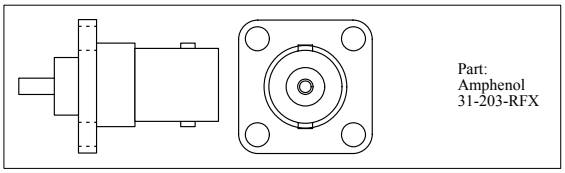
Part:	Quantity: (per assembly)
 Center Piece	1
 Top Plate	1
 Header Cover	1
 Brackets	2

Hole patterns labeled 1 to 11 are for BNC Recptacles
some are optional. Please include the circled:

1 2 3 4 5 6 7 8 9 10 11

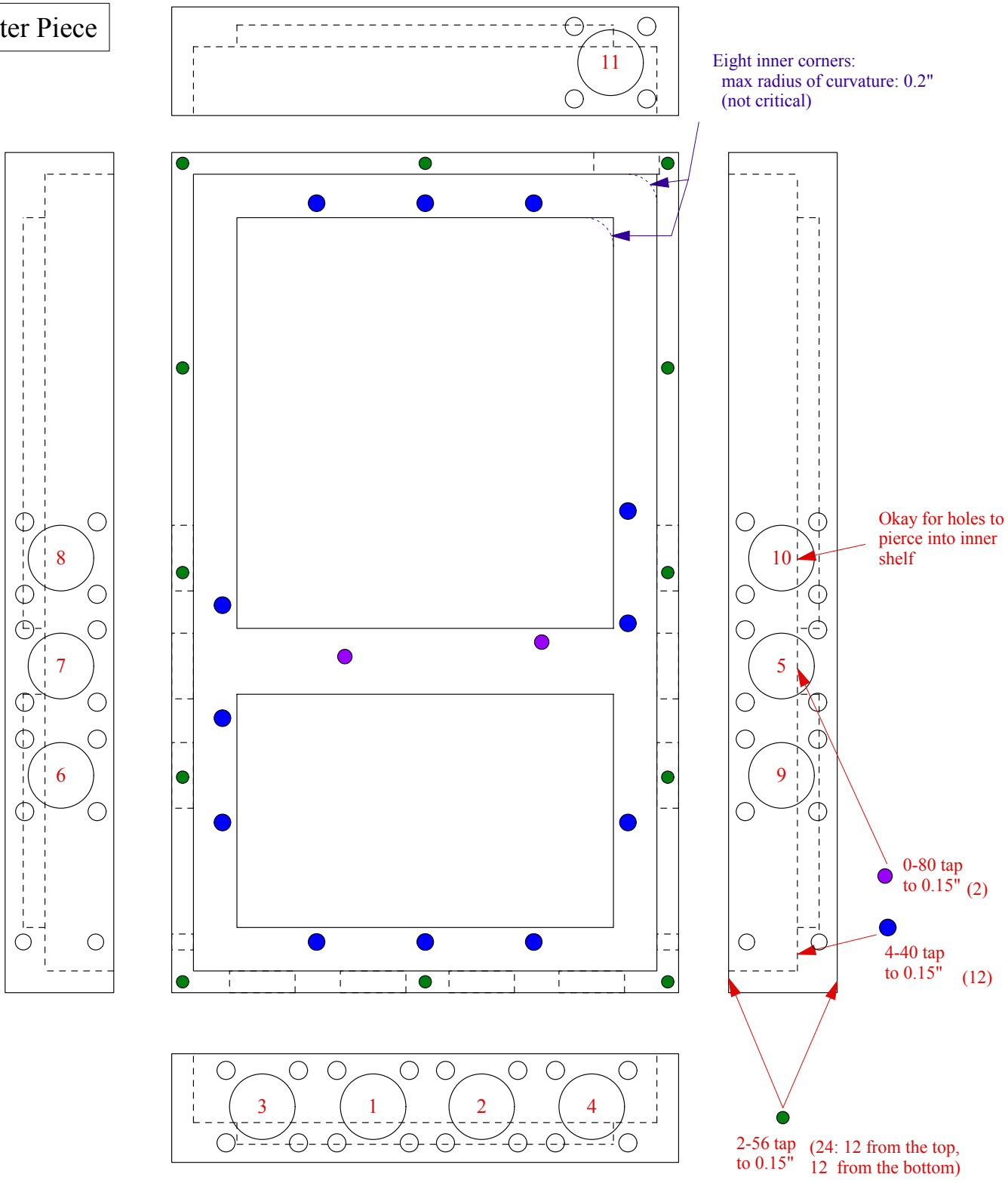
Others are to be omitted.

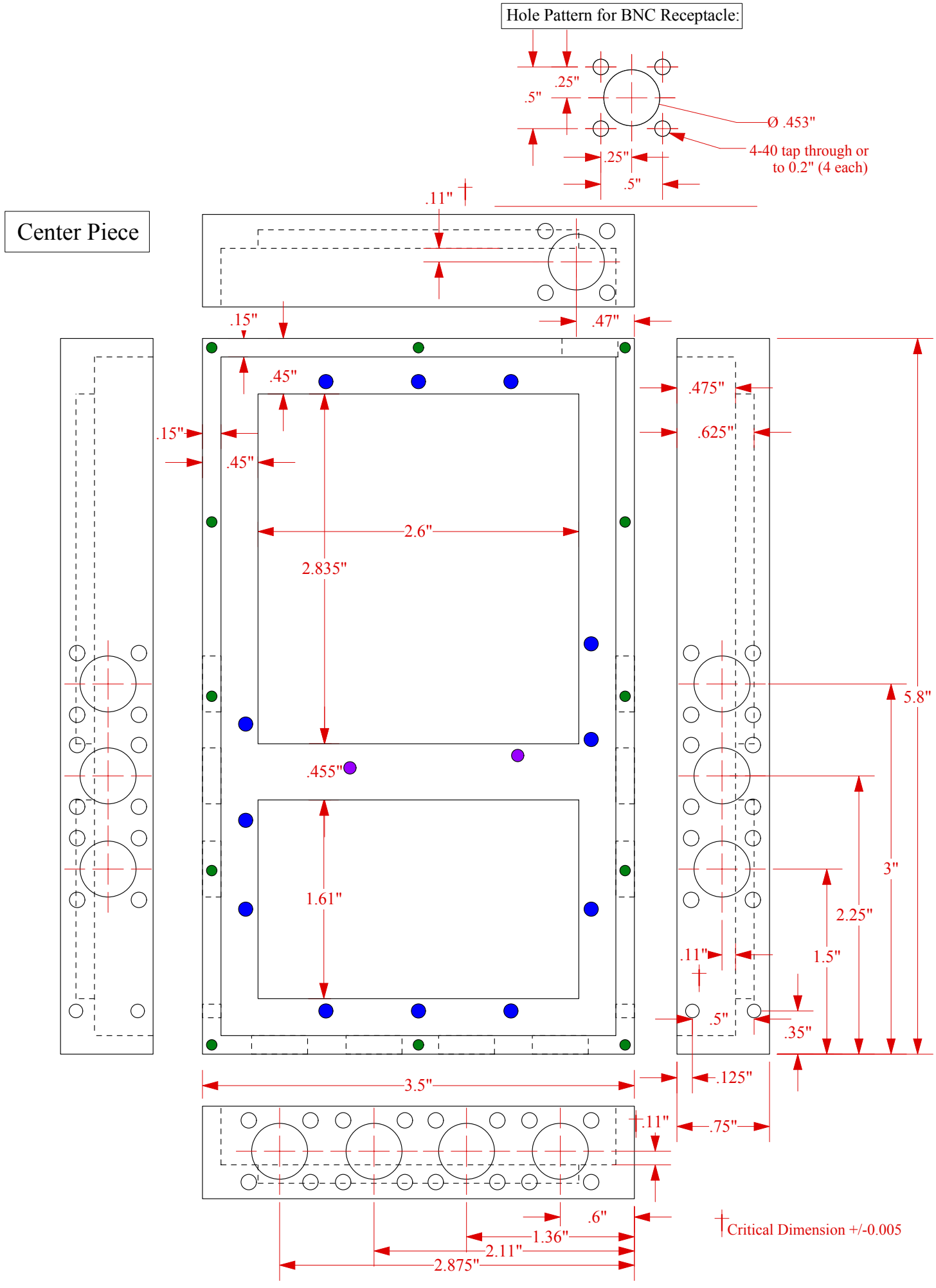
BNC Recptacle



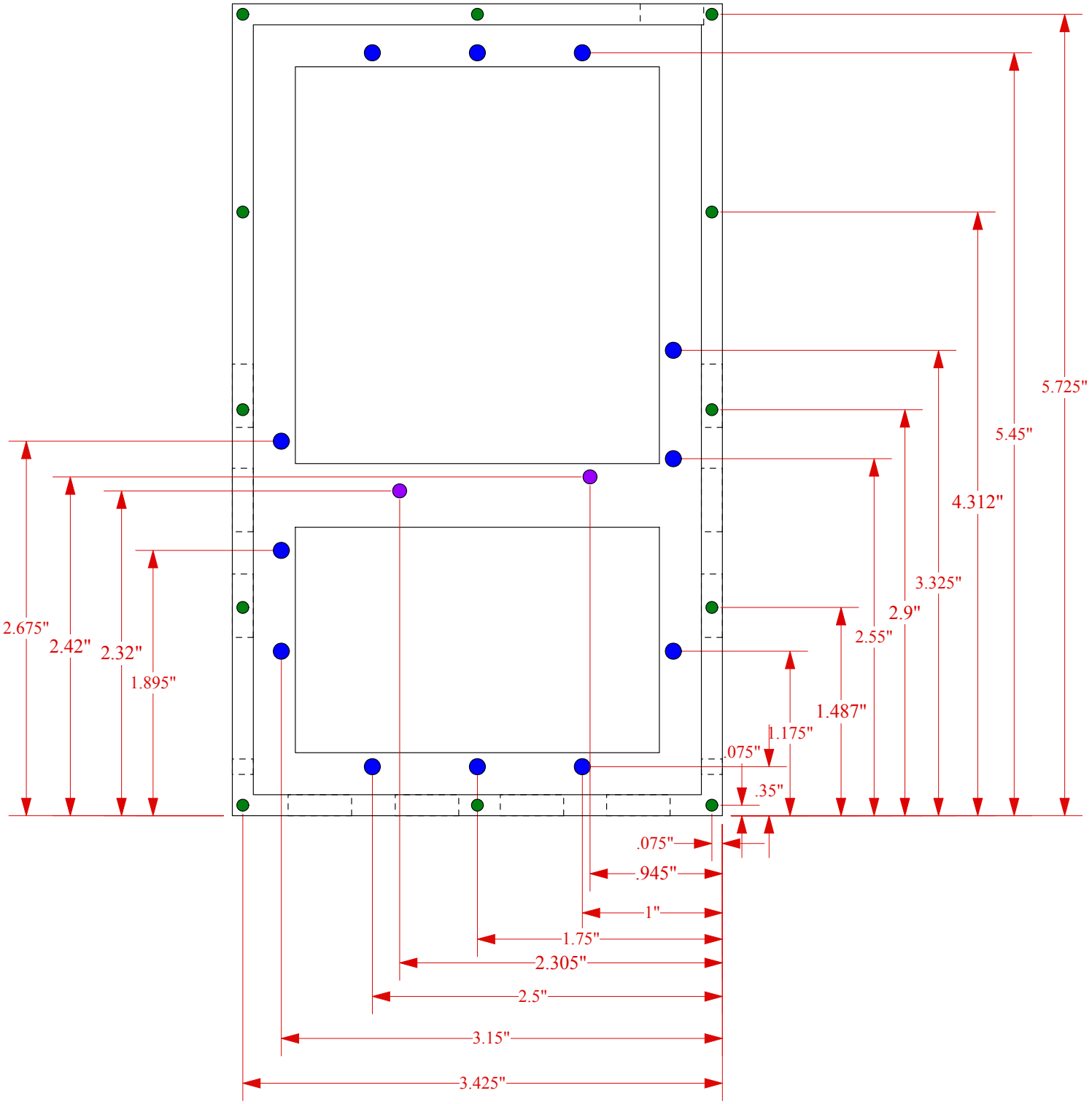
For hole pattern, see dimensioned drawing

Center Piece




Hole Pattern for BNC Receptacle:
.25"
.5"
Ø .453"
4-40 tap through or
to 0.2" (4 each)
.25"
.5"
Center Piece
.11"
.15"
.47"
.45"
.475"
.15"
.625"
.45"
2.6"
2.835"
.455"
1.61"
5.8"
3"
2.25"
1.5"
.11"
.5"
.35"
3.5"
.125"
.11"
.75"
.6"
1.36"
2.11"
2.875"
Critical Dimension +/-0.005

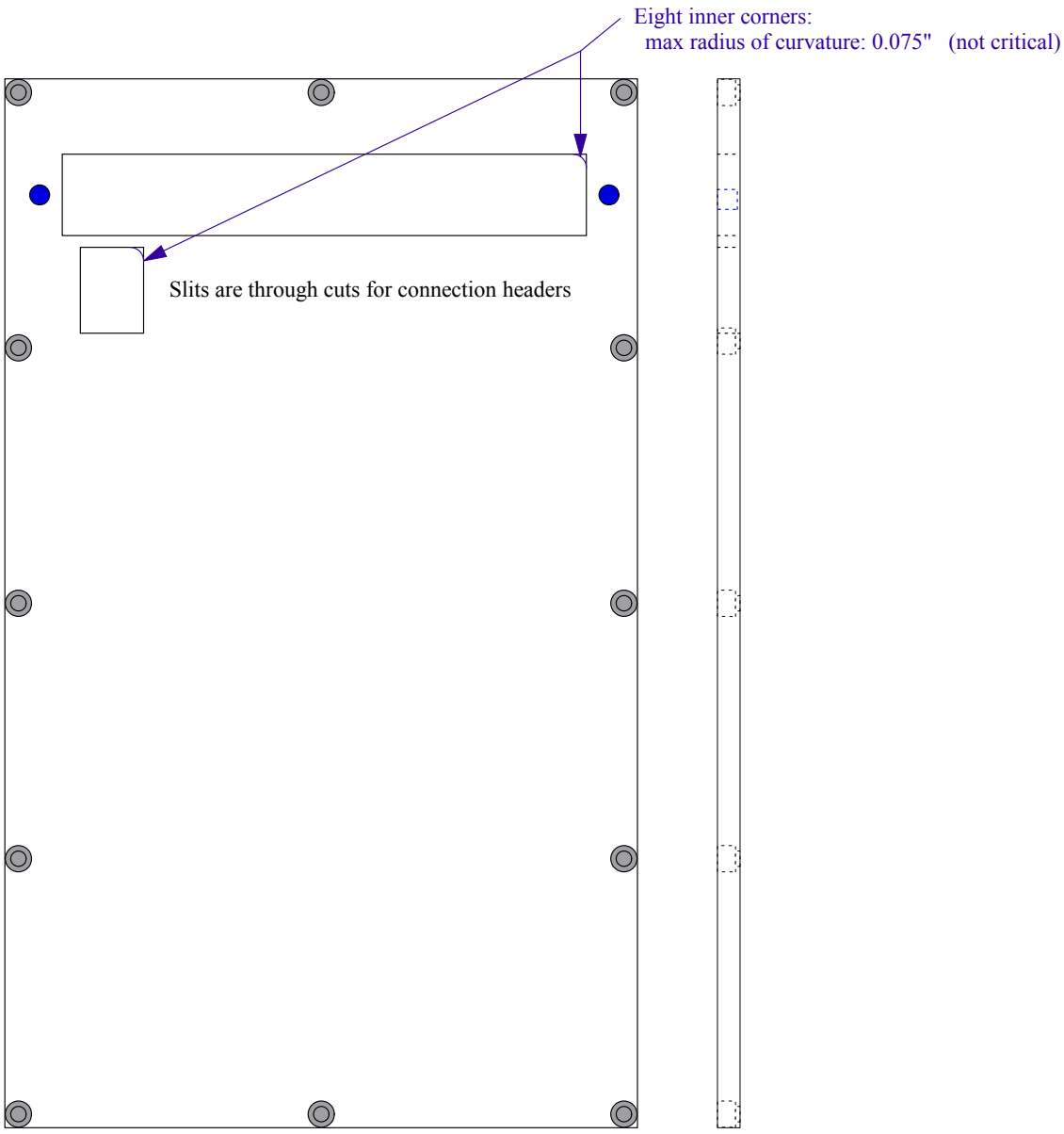
Center Piece



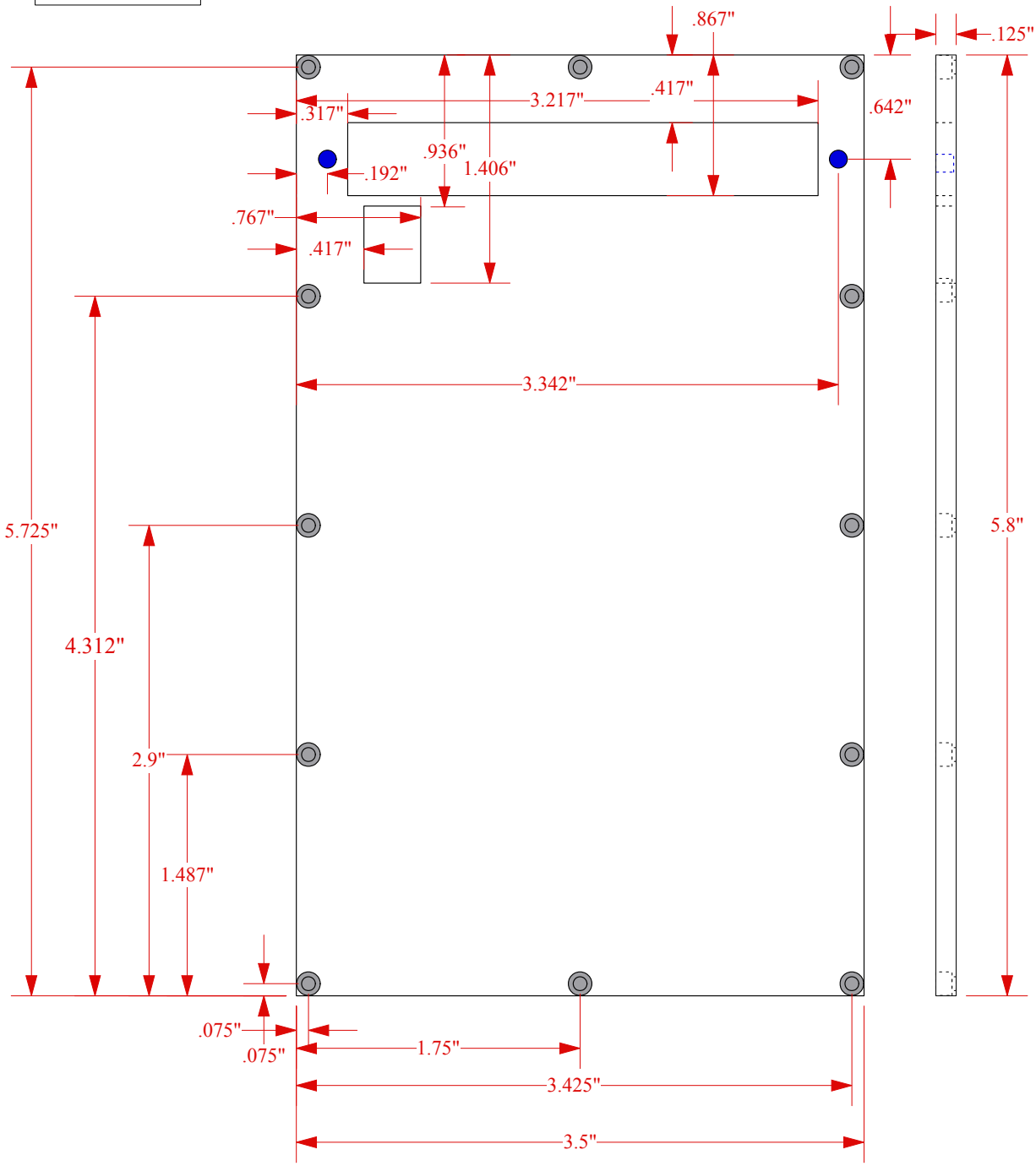
Top Plate

2-56 clearance, counter sunk from top, round hex-head

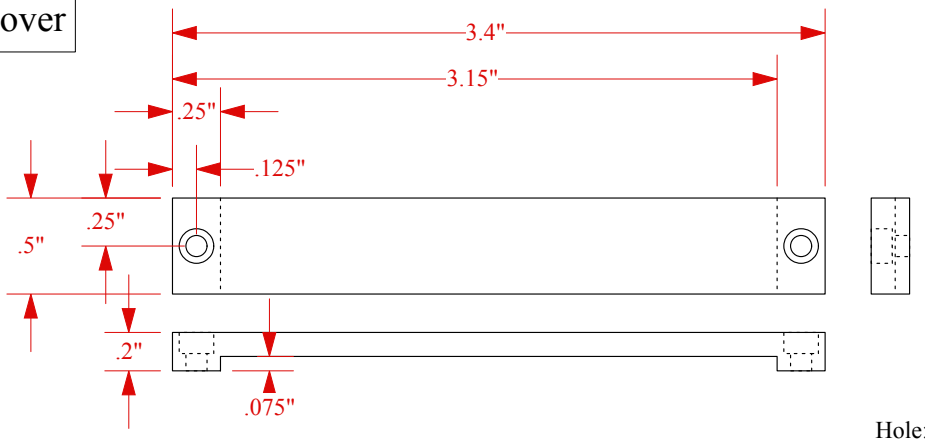
4-40 tap through



Top Plate


.867"
.125"
.317"
3.217"
.417"
.642"
.936"
1.406"
.192"
.767"
.417"
3.342"
5.725"
5.8"
4.312"
2.9"
1.487"
.075"
.075"
1.75"
3.425"
3.5"

Header Cover



Hole: 4-40 clearance, counter sunk from top

Bracket